REMARKS/ARGUMENTS

This Amendment is in response to the Office Action mailed May 24, 2006. Claims 1-3 and 5-17 were pending in the present application. This Amendment amends claims 1, 7, 11, 13, 15, 16, and 17; and cancels claims 3 and 9-10; leaving pending in the application claims 1-2, 5-8 and 11-17. Reconsideration of the rejected claims is respectfully requested.

I. Rejection under 35 U.S.C. §112

Claims 1-3 and 5-17 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, claims 1, 7, and 13 are rejected as failing to indicate which of the elements provides the storing function. Although Applicants do not necessarily agree with the rejection, these claims as amended recite that the control logic assigns each of multiple data bursts for a request to a respective buffer in the memory interface, and the memory interface then stores the data for each burst in the respective buffer. As such, claims 1, 7, and 13, and the claims that depend therefrom, should be sufficiently definite. Applicants therefore respectfully request that the rejection with respect to claims 1-3 and 5-17 be withdrawn.

II. Rejection under 35 U.S.C. §103

(a) *Gray* and *Becker*

Claims 1-3, 7-10, 13-14, and 16 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* (U.S. Pat. No. 6,816,923) in view of *Becker* (U.S. Pat. No. 6,950,884). Applicants respectfully submit that these references do not teach or suggest each element of these claims.

For example, Applicants' claim 1 as amended recites a memory controller, comprising:

> at least one bus interface, each bus interface being for connection to at least one respective device for receiving memory access requests;
> **a memory interface, for connection to a memory device over a memory bus;**
> **a plurality of buffers in the memory interface;** and
> control logic, for placing received memory access requests into a queue of memory access requests,

PAGE 9/14 * RCVD AT 8/22/2006 1:41:09 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/8 * DNIS:2738300 * CSID:415 576 0300 * DURATION (mm-ss):05-54

> **wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, each of said multiple data bursts is assigned by the control logic to a respective buffer** of the plurality buffers in the memory interface, and **data from each of said multiple data bursts is stored by the memory interface in the respective buffer, and**
>
> **wherein, for a wrapping memory access request requiring multiple buffers, data required for a beginning and an end of the wrapping memory access request are assigned to a single respective buffer by the control logic and stored concurrently in the single respective buffer by the memory interface**

(*emphasis added*). In this claimed embodiment, a single request is received from a device over a bus interface, that single request for a single device requiring multiple data bursts over the memory bus from a single memory device. For this request, the control logic assigns each of the data bursts for the single request to one of the buffers in the memory interface. The single request can be a wrapping request, meaning that "data to be read from the memory device is stored at memory locations in the memory device, with the addresses of those memory locations returning to near the start point towards the end of the read operation" (Applicants' specification page 2, lines 2-6). In a system of the prior art, this would result in "only a part of the data returned from the memory device in the first data burst [being] passed to the requesting device, and that the same burst is requested again at the end of the read operation to allow the remaining data to be passed to the requesting device" (spec. p. 2, lines 8-13). In claim 1, however, the data for the wrapping memory request is assigned and stored such that data required for a beginning and end of the single wrapping memory request are assigned to a single respective buffer by the control logic and stored concurrently in the single respective buffer (the data for the end of the request is stored in the remaining portion of the first buffer storing data for the beginning of the request (spec. p. 2, lines 20-33)). This prevents the need for an additional request to go back and get the data for the end of the request, thereby increasing the available bandwidth. Such limitations are neither disclosed nor suggested by *Gray* and *Becker*, either alone or in combination.

For example, *Gray* teaches a direct memory access (DMA) system including a DMA engine that includes a data reservoir having a number of memory buffers in order to consolidate memory buffers for the various devices into the DMA reservoir, the reservoir including portions that correspond to different devices (col. 2, lines 34-47; col. 3, line 64-col. 4, line 18). The use

PAGE 10/14 * RCVD AT 8/22/2006 1:41:09 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/8 * DNIS:2738300 * CSID:415 576 0300 * DURATION (mm-ss):05-54

of the consolidated memory reservoir also provides the ability to centralize addressing and provide each device with data in a timely manner and with increased bandwidth (col. 2, lines 34-56). *Gray* does not teach or suggest a memory interface including a plurality of buffers as recited in Applicants' claim 1, as *Gray* consolidates memory into buffers in the data reservoir and does not utilize buffers in a memory interface, instead teaching replacing buffers for individual devices with the reservoir (shown in Fig. 3; also col. 2, lines 34-47; col. 4, lines 10-12).

Further, *Gray* does not teach or suggest control logic for assigning multiple bursts for a single request to a plurality of buffers in a memory interface. *Gray* includes a plurality of different device-specific buffers in the DMA engine, so that requests for separate devices are sent to separate buffers (Fig. 3; col. 8, lines 10-21). *Gray* does not teach or suggest different buffers for different portions of a single request from a single device as recited in Applicants' claim 1. Further, as recognized in the Office Action on page 4, *Gray* does not teach or suggest a request requiring multiple data bursts and a wrapping memory access request requiring multiple buffers, with data required for a beginning and an end of the request being stored in a single buffer. For at least these reasons, *Gray* cannot render obvious Applicants' claim 1 or the claims that depend therefrom.

Becker does not make up for the deficiencies in *Gray* with respect to Applicants' claim 1. *Becker* teaches a DMA device for transferring data between two processors (col. 1, lines 54-60; col. 4, lines 32-58). *Becker* teaches using "cyclic memories," wherein read and write access between the two processors always takes place in rising or falling memory block order (col. 8, line 65-col. 9, line 6). For example, when the last block of one control information memory is reached, the first block is automatically written to as the next memory block (col. 8, line 65-col. 9, line 6). There is no teaching or suggestion in *Becker*, however, that data needed for the beginning and end of a single request are stored concurrently in a single buffer as recited in Applicants' claim 1. *Becker* re-uses buffers in a cyclical fashion (writing, then subsequently writing over blocks), but does not teach wrapping requests as recited in Applicants' claim 1. Further, *Becker* teaches writing in a cyclical order but does not teach or suggest writing the ending portion of any data in the remaining portion of a first buffer used to store the data,

PAGE 11/14 * RCVD AT 8/22/2006 1:41:09 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/8 * DNIS:2738300 * CSID:415 576 0300 * DURATION (mm-ss):05-54

concurrently with the beginning portion. *Becker* only stores subsequent data in a buffer when the previous data is flagged to be overwritten (bits such as e_si_5 and e_si_6 have value 0), and thus cannot be part of the same request data (col. 5, lines 40-49). Therefore, *Becker* cannot render obvious Applicants' claim 1 or the claims that depend therefrom.

Further, there would be no motivation to combine *Gray* and *Becker*. The Office Action states on page 5 that it would have been obvious to include *Becker's* circular buffer for buffering the transfer of multiple data bursts into each of *Gray's* device buffers, but it is respectfully submitted that *Gray* has buffers that are specific to each device, so writing in a circular fashion to different buffers would not be of any benefir as a request from a device must go to a specific buffer. Further, since a purpose of *Gray* is to address latency issues, it would not make sense to write to the device-specific buffers in a cyclical manner, as a given device might not have a request pending, or a device might have to wait for all other devices to request before being able to request.

For at least these reasons, the combination of *Gray* and *Becker* fails to teach or suggest each element of Applicants' claim 1 as amended, such that these references cannot render obvious Applicants' claim 1 or the claims that depend therefrom. Independent claims 7 and 13 recite limitations that similarly are not rendered obvious by these references for reasons including those cited above. Applicants therefore respectfully request that the rejection with respect to claims 1-3, 7-10, 13-14, and 16 be withdrawn.

(b) *Gray, Becker,* and *Kuronuma*

Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* and *Becker*, and further in view of *Kuronuma* (U.S. Pat. No. 6,859,848). Claims 5 and 11 depend from claims 1 and 7, respectively, which are not rendered obvious by *Gray* and *Becker* as discussed above. *Kuronuma* does not make up for the deficiencies in *Gray* and *Becker* with respect to these claims. *Kuronuma* teaches a memory control system for sequentially accessing an arbitrary address in an SDRAM circuit (col. 4, lines 22-25), and is cited as teaching sequential access to an SDRAM (OA pages 7-8). *Kuronuma* does not, however, teach or suggest data

PAGE 12/14 * RCVD AT 8/22/2006 1:41:09 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/8 * DNIS:2738300 * CSID:415 576 0300 * DURATION (mm-ss):05-54

required for a beginning and an end of a single wrapping memory access request being assigned to a single respective buffer by control logic and stored concurrently in the single respective buffer by the memory interface. As such, *Kuronuma* cannot render obvious claims 1 and 7, or dependent claims 5 and 11, alone or in any combination with *Gray* and *Becker*. Applicants therefore respectfully request that the rejection with respect to claims 5 and 11 be withdrawn.

(c) *Gray, Becker, and Microsoft*

Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* and *Becker*, and further in view of *Microsoft* ("Microsoft Computer Dictionary", 2002 p. 469). Claims 6 and 12 depend from claims 1 and 7, respectively, which are not rendered obvious by *Gray* and *Becker* as discussed above. *Microsoft* does not make up for the deficiencies in *Gray* and *Becker* with respect to these claims. *Microsoft* is cited as teaching SDRAM as a common type of RAM (OA pages 9). *Microsoft* does not, however, teach or suggest data required for a beginning and an end of a single wrapping memory access request being assigned to a single respective buffer of a memory interface by control logic and stored concurrently in the single respective buffer by the memory interface. As such, *Microsoft* cannot render obvious claims 1 and 7, or dependent claims 6 and 12, alone or in any combination with *Gray* and *Becker*. Applicants therefore respectfully request that the rejection with respect to claims 6 and 12 be withdrawn.

(d) *Gray, Becker, and Nguyen*

Claims 15 and 17 (please note typo in OA p. 9) are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* and *Becker*, and further in view of *Nguyen* (U.S. Pat. No. 5,335,326). Claims 15 and 17 depend from claims 1 and 7, respectively, which are not rendered obvious by *Gray* and *Becker* as discussed above. *Nguyen* does not make up for the deficiencies in *Gray* and *Becker* with respect to these claims. *Nguyen* teaches a FIFO bus (col. 1, line 59-col. 2, line 22), and is cited as teaching a FIFO buffer flow regulation system (OA page 10). *Nguyen* does not, however, teach or suggest data required for a beginning and an end of a single wrapping memory

PAGE 13/14 * RCVD AT 8/22/2006 1:41:09 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/8 * DNIS:2738300 * CSID:415 576 0300 * DURATION (mm-ss):05-54

access request being assigned to a single respective buffer of a memory interface by control logic and stored concurrently in the single respective buffer by the memory interface. As such, *Nguyen* cannot render obvious claims 1 and 7, or dependent claims 15 and 17, alone or in any combination with *Gray* and *Becker*. Applicants therefore respectfully request that the rejection with respect to claims 15 and 17 be withdrawn.

III. Amendment to the Claims

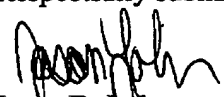
Unless otherwise specified, amendments to the claims are made for purposes of clarity, and are not intended to alter the scope of the claims or limit any equivalents thereof. The amendments are supported by the specification and do not add new matter.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



Jason D. Lohr
Reg. No. 48,163

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
JDL:km
60799076 v1

PAGE 14/14 * RCVD AT 8/22/2006 1:41:09 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/8 * DNIS:2738300 * CSID:415 576 0300 * DURATION (mm-ss):05-54